VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

Please Amend the Title as follows:

THIN FILM SEMICONDUCTOR PACKAGE [AND METHOD OF FABRICATION] UTILIZING A GLASS SUBSTRATE WITH COMPOSITE POLYMER/METAL INTERCONNECT LAYERS

Please Amend the Specification, page 4, under DESCRIPTION OF DRAWINGS as follows:

Figs. [4a-4j] 4a-4l show a fourth embodiment of the invention and the major fabrication steps.

Figs. [5a-5j] 5a-5l show a fifth embodiment of the invention and the major fabrication steps.

Please Amend the Specification, page 7, paragraphs two and three as follows:

Multiple alternating layers of dielectric and metal (not shown) may be deposited and patterned until the final layer of dielectric 26 is then deposited, on the last layer of metal 24, and holes opened 27 to the contact points of metal layer.

A layer of solder is deposited by electroplating, screen printing or ball mounting and contacts are made through the etched holes in the insulating layer to the final metal layer. The solder is then reflowed to form the solder bumps 28. Alternately, gold bumps[, or pins] may be used, as is known in the art.

In the Claims:

Please Amend Claim 39 as follows:

39. (AMENDED) A method for fabricating a thin film semiconductor die package, comprising the steps of:

providing a planar glass substrate;

attaching semiconductor dies to said planar glass

substrate;

[sequentially depositing one or more polymer layers and one or more metal interconnect layers over said substrate;]

forming a polymer layer overlying said planar glass substrate and filling gaps between said semiconductor die;

thereafter depositing a dielectric layer overlying said polymer layer and said semiconductor die;

patterning said dielectric layer to form openings to said semiconductor die;

forming a metal interconnect layer overlying said dielectric layer and contacting said semiconductor die;

forming a layer of solder over and connected to said [one or more] metal interconnect layer [layers]; and

reflowing the solder to form solder bumps.

Please Cancel Claim 40.

Please Amend Claim 41 as follows:

41. (AMENDED) A method of fabricating [the] a thin film semiconductor die package structure comprising:

providing a metal substrate;

forming a patterned glass layer overlying said metal substrate wherein said patterned glass layer has openings exposing said metal substrate; [with cavities for mounting semiconductor dies on said metal substrate;]

attaching semiconductor die to said exposed metal substrate;

[sequentially forming polymer insulating layers and metal interconnect layers;]

depositing a dielectric layer overlying said patterned glass layer and said semiconductor die;

patterning said dielectric layer to form openings to said semiconductor die;

forming a metal interconnect layer overlying said dielectric layer and contacting said semiconductor die;

forming a layer of solder over and connected to said metal interconnect layer; and

reflowing the solder to form solder bumps.

Please Amend Claim 42 as follows:

42. (AMENDED) A method of fabricating a thin film semiconductor die package structure comprising:

providing a first glass substrate with semiconductor dies mounted on said first glass substrate wherein the active surface of said semiconductor dies is facing said first glass substrate;

filling polymer or epoxy between and over the backside of said semiconductor dies [to obtain a planarized surface];

grinding the planarized surface and said backside of said semiconductor dies[, to a desired thickness of said semiconductor dies];

mounting a second glass substrate on the backside of the semiconductor dies;

grinding the first glass substrate [to a desired glass thickness];

etching holes in said first glass substrate to expose said semiconductor dies;

sequentially forming polymer insulating layers and metal interconnect layers over said first glass substrate;

depositing a layer of solder over and connected to a topmost said metal interconnect layer; and

reflowing the solder to from solder bumps.

Please Cancel Claims 43 and 44.

Please Amend Claim 49 as follows:

49. (AMENDED) The method of claim 42 wherein the solder bumps are connected to said interconnect metal and are further incorporated as interconnects to the next level of assembly.

Please Cancel Claim 50.

Please Amend Claim 53 as follows:

53. (AMENDED) A method of fabricating a thin film semiconductor die package structure comprising:

providing a first glass substrate with semicondutor dies mounted on said first glass substrate wherein the active surface of said semiconductor dies is facing said first glass substrate;

filling polymer or epoxy between and over the backside of said semiconductor dies, to obtain a planarized surface;

grinding the planarized surface, and said backside of said semiconductor dies[, to a desired thickness of said semiconductor dies];

mounting a second glass substrate on the backside of the semiconductor dies;

removing said first glass substrate;

sequentially forming polymer insulating layers and metal interconnect layers over said semiconductor dies;

depositing a layer of solder over and connected to a topmost said metal interconnect layer; and

reflowing the solder to form solder bumps.

Attachment A

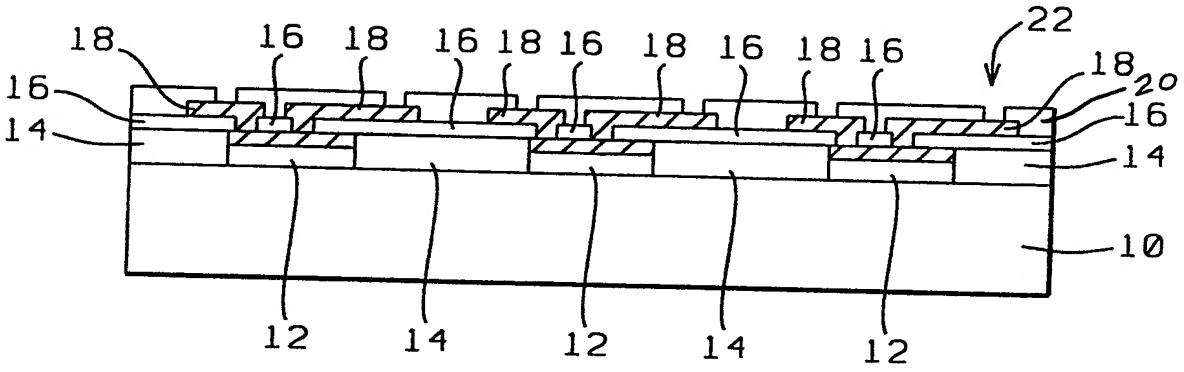


FIG. 1e

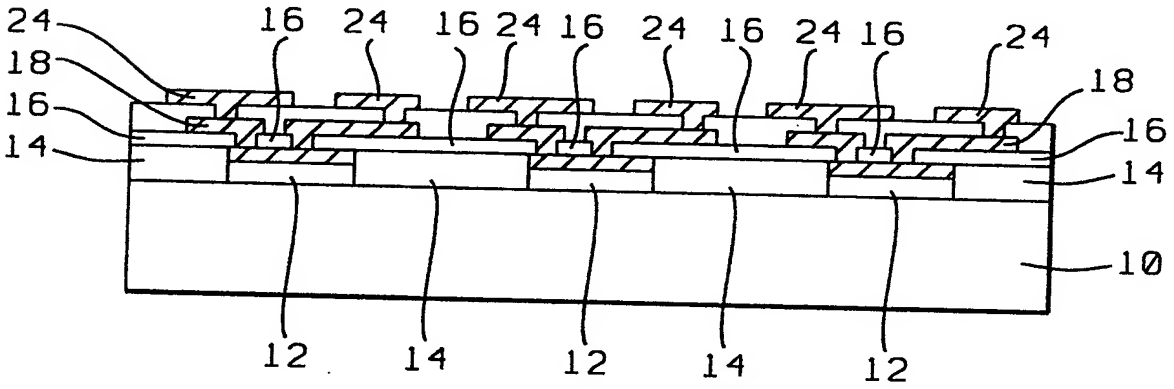


FIG. 1f

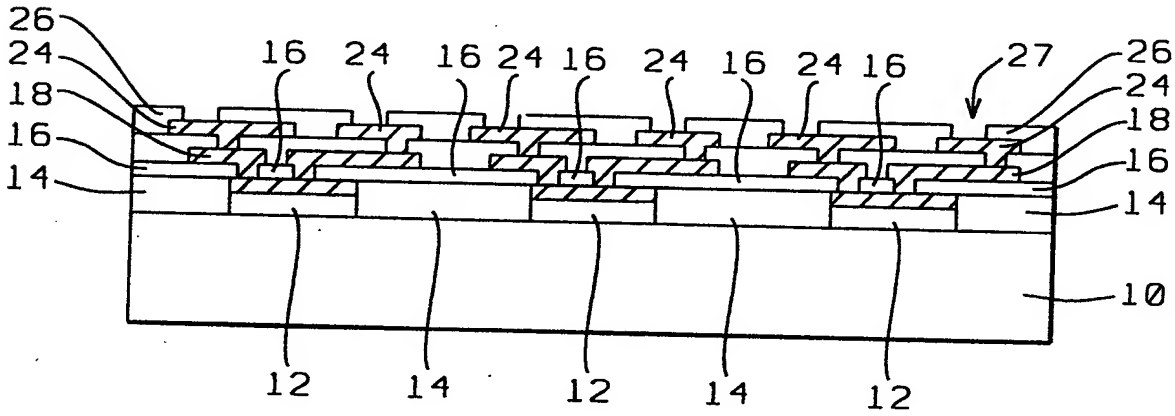


FIG. 1g

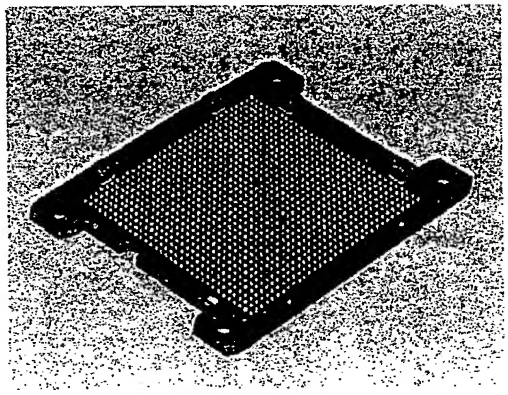
Attachment B

CIN::APSE®

High-Speed Interconnect Technology

Features

- High signal speed capability enabling frequencies greater than 20 GHz.
- Z-Axis, solderless, compression mount interconnect system.
- Applications include production Land Grid Array (LGA) integrated circuit sockets, flex circuit to PCB, and parallel PCB to PCB interconnections.
- Provides solutions to many of the problems associated with through hole and surface mount soldered technology.
- Enables upgrade and system maintenance strategies.
- Available in custom I/O counts to over 1,000 as well as offering unique contact patterns that facilitate shortening of signal paths.
- Offers low profile capabilities with compressed signal path length as short as 0.8 mm.
- Contact centerline spacing of 1mm or greater.
- Excellent reliability in commercial, military, and aerospace applications.
- Application can result in lower installed and system maintenance costs.



Materials
Contact Material: Molybdenum
CIN::APSE® Contact Plating: Gold
Plunger Material: Copper alloy
Plunger Plating: Gold
Insulator Material: Liquid crystal polymer
Packaging Tray Material: Anti-static ABS

Environmental
Button-Only Configuration with 0.020" (0.5 mm) diameter
Temperature Life Testing: 1000 Hours @ 200°C
Thermal Shock: 2000 Cycles @ -20°C to +85°C
Humidity: 5000 Hours @ 30°C to 80°C, 85% RH
Salt Spray: 96 Hours
Low Temperature: Operates in liquid nitrogen (77°K)
Bellcore TR-NWT-001217: Passed with plungers

Electrical
Button-Only Configuration with 0.020" (0.5 mm) diameter
DC Resistance: 15 milliohm average
Inductance: Less than 1 nH
Current-Carrying Capability: 1-3 Amps
Insulation Resistance: 25,000 Megohm @ 500 VDC
Dielectric Withstanding Voltage: 900 VAC at sea level

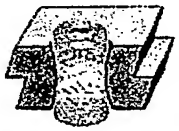
Mechanical
Button-Only Configuration with 0.020" (0.5 mm) diameter
Durability: 25,000 Z-axis actuations (CIN::APSE® contact only)
Shock: 100 Gs; 6 milliseconds, no discontinuity greater than 2 nanoseconds
Vibration: 20 Gs; 10-20,000 Hz; no discontinuity greater than 2 nanoseconds

What is CIN::APSE®?
CIN::APSE® is a solderless z-axis interconnect technology that offers exceptional mechanical and electrical performance. CIN::APSE® is a proven technology that has a ten year record of providing reliable solutions to some of the most demanding applications. Custom made to meet your specific needs, CIN::APSE® utilizes a multipoint contact that can be as small as .8mm in height, comes in 1mm centers, and can handle signal frequencies greater than 20 Ghz.

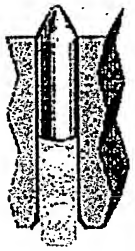
The key to this high performance technology is the CIN::APSE® button-contact. The contacts are made by randomly winding gold plated molybdenum or tungsten wire into a cylindrical button. The buttons are then loaded(stitched) into a custom molded insulator configured to the exact requirements of the application. Cinch's patented hourglass shaped button-hole allows the button to float and, therefore, stay in contact even under extreme Thermal Expansion(TCE) mismatch between mated substrates.

Unlike other z-axis technologies, such as elastomeric connectors, CIN::APSE® buttons have a high modulus of elasticity which means they can be compressed thousands of times without taking a compression set. CIN::APSE® buttons are also very lightweight and thermally stable which makes them extremely resistant to intermittent signals caused by shock/vibration or thermal cycling.

Product Offerings
CIN::APSE® is more than a connector; it's a versatile technology. By using our many different sizes of buttons, plungers and spacers we can create an almost limitless number of configurations. This flexibility means that you can design CIN::APSE® to meet your exact interconnect needs.

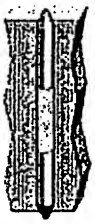


Button Only: This is the basic CIN::APSE® contact configuration. It is ideally suited for applications requiring minimum height, high density, and signal integrity. This configuration is used in LGA sockets.



Plunger-Button: The addition of a gold plated brass plunger increases the durability of the CIN::APSE® contact while also achieving additional height. This configuration is ideally suited for board-to-board applications and those that require excessive handling.

Plunger-Button-Plunger: Adding a second plunger to the connector results in the most durable and tallest system. This configuration is best suited where both sides of the contact will see excessive handling.



Button-Spacer-Button: Using two buttons with a gold plated brass spacer in between creates a connector with all the benefits of the button only style, but the ability to span greater z-axis heights. This configuration is used where the button's multiple points of contact are needed.

Connector Type	Mated Height
Button Only (.015" dia. button)	.025"
Button Only (.020" dia. button)	.032" to .050"
Button Only (.040" dia. button)	.032" to .075"
Plunger-Button	.078" to .50"
Plunger-Button-Plunger	.120" to 1.50"
Button-Spacer-Button	.100" to 1.00"

Guidelines for using CIN::APSE® connectors

Here are some guidelines to follow when laying out your PCB, flex circuit, chip package or MCM.

	.020" dia. button				.040" dia. button
Characteristics	**Button Only**	**Button/ Plunger**	**Plunger/ Button/ Plunger**	**Button/ Spacer/ Button**	**Button Only**
Pad Size (min. dia.)	.030"	.030"	.020"	.030"	.060"
Minimum Center Spacing	1mm	.050"	.050"	.050"	.070"
Circuit Resistant (milli-Ohms)	10-15	30-35	45-50	40-45	5-10
Inductance (nano-Henry)	<1	<1	<2	<1	<1
Min. Compression Force/button	2 oz.	2 oz.	2 oz.	4 oz.	4 oz.
Current Carrying Capacity	1-3 A	1-3 A	1-3 A	1-3 A	3-5 A
Contact Travel	up to .010"	up to .010"	up to .010"	up to .020"	up to .012"

Pad Plating: 20µin. Au over 50µin. Ni if multiple cycles are needed (flash Au for single mate)

In-pad vias: < half the diameter of the button

PCB Flatness: .003 in./in.
Pad true position: <.005"

Compression System Design
As stated before, CIN::APSE® is a solderless connector technology, which relies on compression to make contact between components. Therefore, design of a proper compression system for the connector is very important. The compression system must take into account the effects of the following: PCB thickness, connector thickness, number and spacing of buttons, and flatness of the mating surfaces.

Use the common example listed below as a base of reference for your designs.

- For a .062" thick PCB mating to a .020" dia. button-only CIN::APSE® connector on .050" centers, you will need a locking device every 1.5 inches.
- If planarity cannot be of achieved, a stiffener plate must be attached to the opposite side of the PCB to limit substrate bow.
- The plate should be of suitable material and thickness to fit the application.

Cinch has many years of experience in designing compression systems with CIN::APSE®. We can help optimize a compression system to meet your specific application.

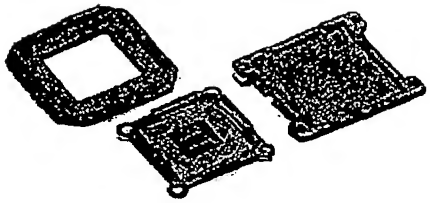
Applications
CIN::APSE® can be used in almost any application where you need a highly reliable interconnect between two parallel surfaces. Common applications include:

-Chip Package-to-Board (commonly called LGA - Land Grid Array)
-Board-to-Board
-Flex-to-Board
-Component-to-Board

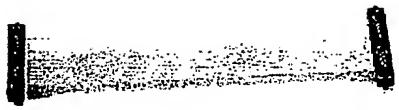
CIN::APSE® connectors are commonly used in a wide variety of markets such as:

- High End Computers (Servers, Workstations, Super Computers, ATE)
- Mil/Aero (RF Antennas, missile guidance, satellites, SEM-E modules)
- Telecommunications (cell phones, portable devices, high speed RF coax, Fiber Optic Transceivers)
- Automotive (sensors, ECU attach)

CIN::APSE® is especially well suited for high speed digital or RF applications. Depending on the configuration, CIN::APSE® can handle 26 Ghz signals with less than 3db of loss. Validating independent test reports and customer written white papers are available.

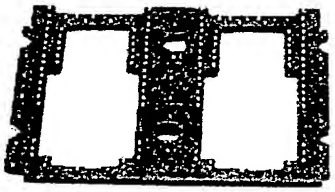


LGA Production IC Sockets



Flex Circuit to PCB

LED to Flex to PCB



Hybrid Circuit to Flex to PCB

For Custom Orders and designs, click here.